Formal Verification of Deadlock Avoidance Mechanisms in Networks-on-Chip

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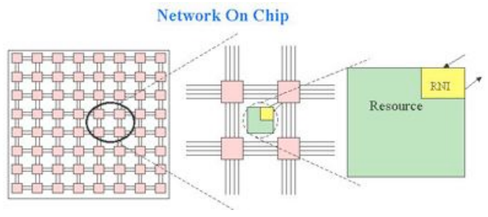
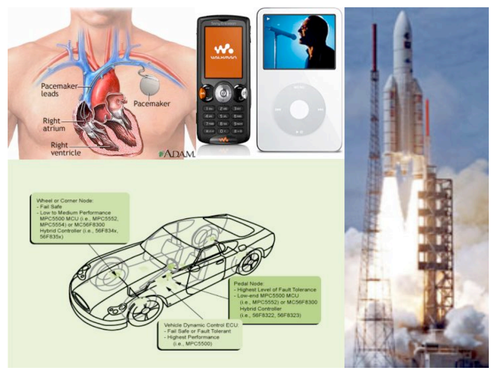
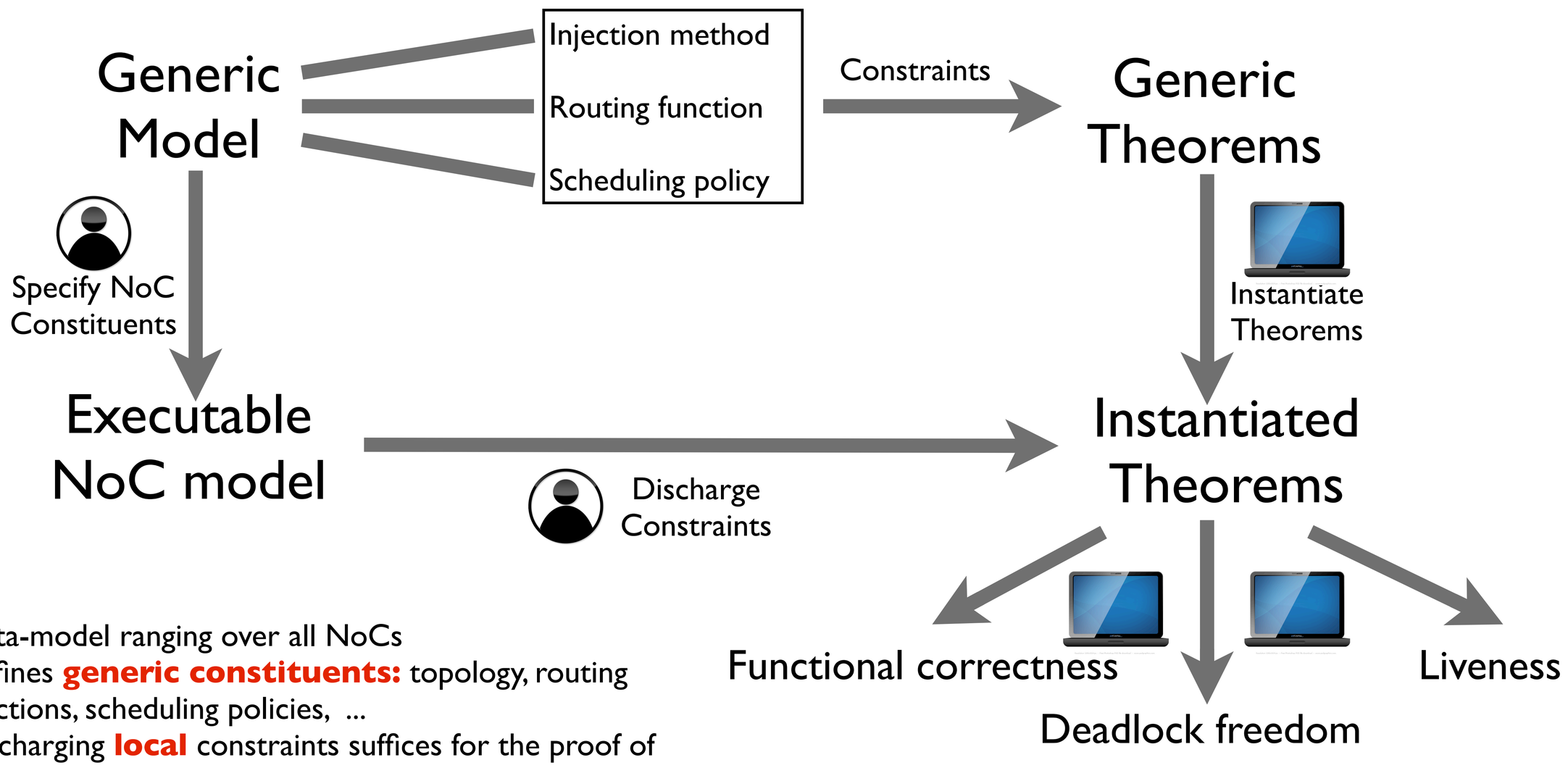
Systems and Networks-on-Chip



- Ubiquitous, safety critical
- Platform-based design: SoC from pre-designed parameterized IPs
- Challenges: (1) abstraction and (2) communications



The GeNoC Verification method



- Meta-model ranging over all NoCs
- Defines **generic constituents:** topology, routing functions, scheduling policies, ...
- Discharging **local** constraints suffices for the proof of **global** properties

Implementation

- ACL2 logic using encapsulation
- Instantiated constraints automatically generated via functional instantiation

Results

- Liveness: Generic Termination Measure
- Deadlock: Formalization of Dally & seitz' condition for deadlock-free routing

Applications

- Determinisic routing algorithms
- Packet and wormhole switching techniques
- 2D Mesh HERMES NoC, XY Routing

Future Work

- Adaptive routing: Formalizing Duato's theory
- Generic NoC injection methods
- GeNoC layered stack from specification level to implementation level

References

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- W.J. Dally and C.L. Seitz. Deadlock-free message routing in multiprocessor interconnection networks. IEEE Transactions on Computers, (36), 1987
- F. Moraes *et al.* "HERMES: An infrastructure for low-area overhead packet-switching network-on-chip" The VLSI Journal 38(1) 2004