Cross-layer deadlock detection in communication fabrics

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Multicore Communication Fabrics

Figure 1. Transistors, frequency, power, performance, and processor cores over time. The original Moore's law projection of increasing transistors per chip remains unabated even as performance has stalled.
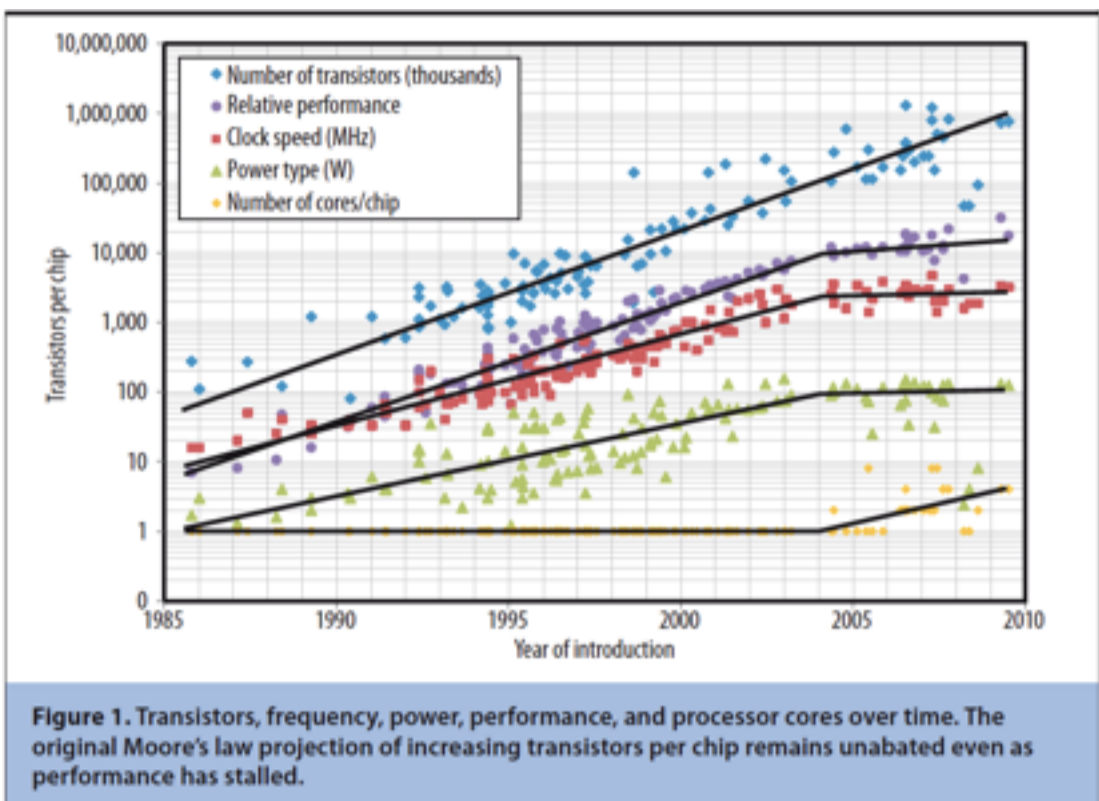
- Moore's law: integration capabilities are still growing fast
- Limited power budget prevents increase of clock speed
- More performance thanks to more cores
- Multi-core communication architectures
  - are key for both performance and correctness
  - are complex and large systems
  - formal methods required for design and verification

Cross-layer Deadlocks

Application layer
- Message types
- Behavior of cores

Network layer
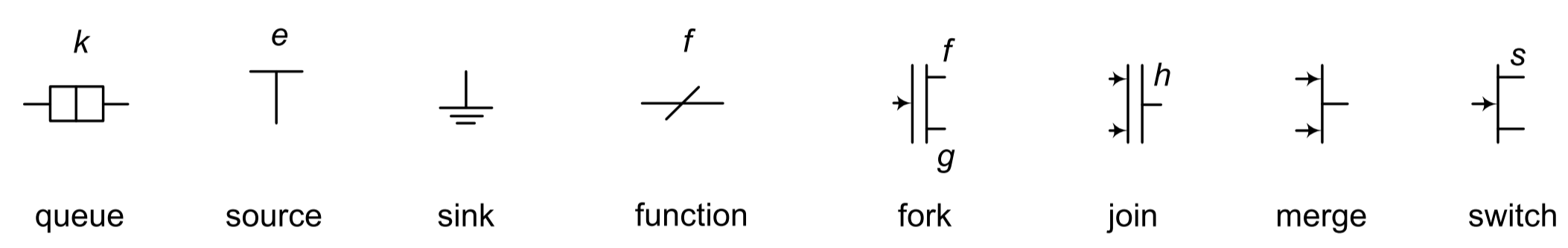- Routing function
- Virtual channels
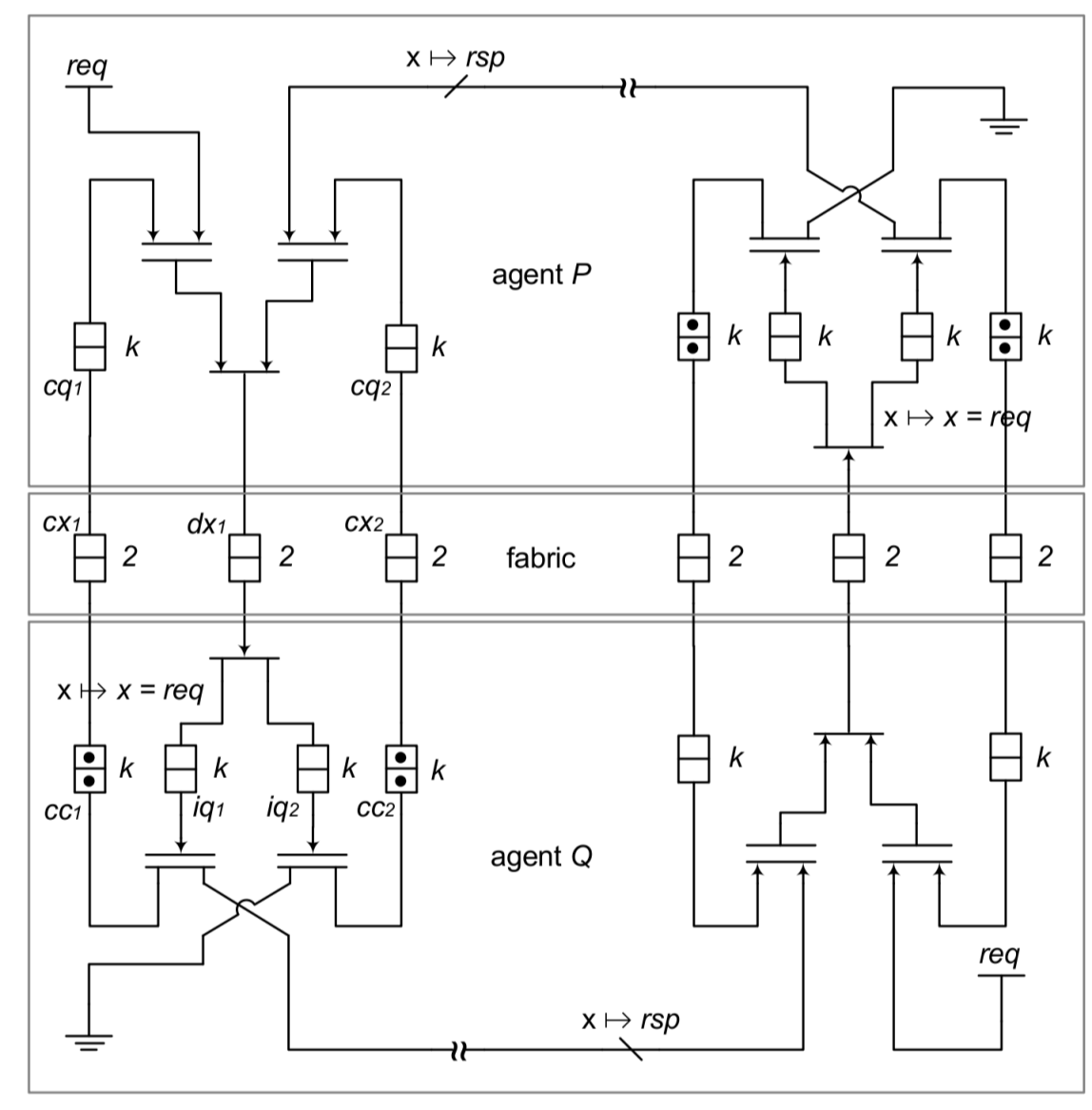
Link layer
- Creditbased flows
- Message counting

Entire System

Deadlocks may emerge from deadlock-free layers

Intel's Description Language

queue   source   sink   function   fork   join   merge   switch

Model-based
  All facets of fabric in one model
Formal
  Accurate semantics for each primitive
Tailored
  High expressivity vs.
  Efficient verification

Results & Applications

2D Mesh
  Request/response message dependencies
  Masters/slaves in various layouts

Spidergon
  Credit-based deadlock prevention
  Write-invalidate cache coherency protocol

See: http://www.cs.ru.nl/~freekver/

Future Work

Formal proof of correctness
  Use earlier work on GeNoC to model and verify our deadlock detection methodology
Lower levels of abstraction
  Translate xMAS to Verilog and formally verify absence of deadlocks on the Verilog code
Hierarchical Verification
  Use composite objects to structure both the model of the communication fabric and its verification

References

- F. Verbeek and J. Schmaltz. *Hunting deadlocks efficiently in micro-architectural models of communication fabrics* (FMCAD '11).
- ----. *Towards the Formal Verification of Cache Coherency at the Architectural Level*. ACM Transactions on Design Automation of Electronic Systems (ACM TODAES).
- ----. *Automatic Generation of Deadlock Detection Algorithms for a Family of Microarchitecture Description Languages of Communication Fabrics* (HLDVT'12).

Acknowledgments

NWO
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(intel)